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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,638	10/17/2003	Toshiaki Saruwatari	1450.1035	1129

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EXAMINER	
LAI, VINCENT	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/686,638	SARUWATARI ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/31/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgment is made of the amendments to the title, abstract, and claims of the application.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 17 October 2003 was considered by the examiner.

4. The information disclosure statement (IDS) submitted on 31 July 2006 was **not** fully considered by the examiner. Copies of the non-patent literature (items AM, AN, and AO) were not submitted and thus not considered.

Continued Examination Under 37 CFR 1.114

5. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3 January 2007 has been entered.

Response to Arguments

6. Applicant's arguments filed 3 January 2007 have been fully considered but they are not persuasive.

Applicant argues, "Krueger fails to teach or even suggest performing a prefetch request *when a branch instruction is decoded*."

Further evidence is given in the rejection below.

Applicant also argues, "Krueger does not mention that the branch target instruction is ignored when a branch does not occur."

Examiner has provided further evidence in the rejection below.

It is also noted that one having ordinary skill in the art would ignore branch target instructions if it were known a branch does not occur. Such implementation prevents data hazards and maintains integrity of data.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 4-6, 9-11, 13-15, 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Krueger et al (U.S. Patent # 6,195,735 B1), herein known as Krueger et al.

As per **claim 1**, Krueger et al discloses an information processing unit, comprising:

a prefetch buffer (See column 8, lines 37-41) prefetching an instruction through a bus with its width being at least twice as large as an instruction length (See column 13, table 2: At least two-times the instruction length is prefetched), to store the prefetched instruction;

a decoder (Decode 42, see figure 1) decoding the instruction stored in said prefetch buffer (See column 5, lines 53-55: Instructions from buffer are decoded);

an arithmetic unit (ALU 142, see figure 4) executing the decoded instruction (See column 17, lines 30-33);

an instruction request control circuit (Access controller 22, see figures 1, 2, and 3) performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded (See figure 4 and column 12, lines 7-14 and column 18, lines 57-

62: The prefetch service block does the actual requesting for prefetches when appropriate. Prefetching is also taught to be able to be done, at the discretion of having ordinary skill in the art, at various stages of the pipeline of figure 4. The pipeline includes a decode stage), otherwise performing the prefetch request sequentially to prefetch instructions (See column 13, lines 13-17: The access controller can either issue an already prefetched instruction or request a prefetch); and

a prefetch control circuit (Prefetch service block 80, see figure 3) prefetching the branch target instruction to said prefetch buffer when a branch is ensured to occur by executing the branch instruction (See column 12, lines 7-14: The prefetch service block does the actual requesting for prefetches when appropriate), while ignoring the branch target instruction when a branch does not occur (See table 2 in column 13: A prefetch is suppressed if a branch is known not to occur).

As per **claim 2**, Krueger et al discloses wherein said prefetch buffer (Instruction fetch 40, see figure 1) prefetches the instruction from a main memory (Main memory 14, see figure 1) through an instruction cache memory (L1 instruction cache 28, see figure 1) (Figure 1 shows the hierarchy and the instruction fetch gets its instructions from the L1 instruction cache, which gets it from main memory).

As per **claim 4**, Krueger et al discloses wherein said prefetch buffer prefetches the instruction from the instruction cache memory through a bus with its width being twice as large as an instruction length (See column 13, table 2: At least two-times the

instruction length is prefetched), and outputs the instruction to said decoder through a bus with its width equal to the instruction length (See column 7, lines 29-32: A single instruction is decoded per cycle).

As per **claim 5**, Krueger et al discloses wherein said prefetch buffer stores four pieces of instructions at maximum (See column 8, lines 37-41: Prefetch buffer are allowed and stores at least 1 instruction, which is less than the maximum).

As per **claim 6**, Krueger et al discloses wherein said decoder and said arithmetic unit perform operations in units of one instruction (See column 7, lines 29-35: A single instruction is decoded per cycle, that decoded instruction being executed during the next cycle).

As per **claim 9**, Krueger et al discloses further comprising a register for writing therein an execution result of said arithmetic unit (Column 7, lines 11-15: Writeback can be to a register).

As per **claim 10**, Krueger et al discloses an information processing method, comprising:

prefetching an instruction through a bus with its width being at least twice as large as an instruction length (See column 13, table 2: At least two-times the instruction length is prefetched), to store the prefetched instruction;

decoding the prefetched instruction (See column 5, lines 53-55: Instructions from buffer are decoded);

executing the decoded instruction (See column 17, lines 30-33);

performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded (See figure 4 and column 12, lines 7-14 and column 18, lines 57-62: The prefetch service block does the actual requesting for prefetches when appropriate. Prefetching is also taught to be able to be done, at the discretion of having ordinary skill in the art, at various stages of the pipeline of figure 4. The pipeline includes a decode stage), otherwise performing the prefetch request sequentially to prefetch the instructions (See column 13, lines 13-17: The access controller can either issue an already prefetched instruction or request a prefetch); and

prefetching the branch target instruction when the branch is ensured to occur by executing the branch instruction (See column 12, lines 7-14: The prefetch service block does the actual requesting for prefetches when appropriate), while ignoring the branch target instruction when a branch does not occur (See table 2 in column 13: A prefetch is suppressed if a branch is known not to occur).

As per **claim 11**, Krueger et al discloses wherein said prefetching an instruction prefetches the instruction from the main memory (Main memory 14, see figure 1) from an instruction cache memory (L1 instruction cache 28, see figure 1) (Figure 1 shows the hierarchy and the instruction fetch gets its instructions from the L1 instruction cache, which gets it from main memory).

As per **claim 13**, Krueger et al discloses wherein said prefetching an instruction prefetches the instruction from the instruction cache memory through a bus with its width being twice as large as an instruction length (See column 13, table 2: At least two-times the instruction length is prefetched), and outputs the instruction to said decoding through a bus with its width equal to the instruction length (See column 7, lines 29-32: A single instruction is decoded per cycle).

As per **claim 14**, Krueger et al discloses wherein said prefetching an instruction stores four pieces of instructions at maximum (See column 8, lines 37-41: Prefetch buffer are allowed and stores at least 1 instruction, which is less than the maximum).

As per **claim 15**, Krueger et al discloses wherein said decoding and said executing perform operations in units of one instruction (See column 7, lines 29-35: A single instruction is decoded per cycle, that decoded instruction being executed during the next cycle).

As per **claim 18**, Krueger et al discloses further said execution step writes an execution result to a register (Column 7, lines 11-15: Writeback can be to a register).

As per **claim 19**, Krueger et al discloses an information processing method, comprising:

prefetching an instruction through a bus with its width being at least twice as large as an instruction length, and storing the prefetched instruction (See column 13, table 2: At least two-times the instruction length is prefetched);

performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded (See figure 4 and column 12, lines 7-14 and column 18, lines 57-62: The prefetch service block does the actual requesting for prefetches when appropriate. Prefetching is also taught to be able to be done, at the discretion of having ordinary skill in the art, at various stages of the pipeline of figure 4. The pipeline includes a decode stage), otherwise performing the prefetch request sequentially to prefetch instructions (See column 13, lines 13-17: The access controller can either issue an already prefetched instruction or request a prefetch); and

prefetching the branch target instruction to said prefetch buffer when a branch is ensured to occur by executing the branch instruction (See column 12, lines 7-14: The prefetch service block does the actual requesting for prefetches when appropriate), while ignoring the branch target instruction when a branch does not occur (See table 2 in column 13: A prefetch is suppressed if a branch is known not to occur).

As per **claim 20**, Krueger et al discloses an information processing apparatus, comprising:

means for prefetching and storing an instruction through a bus with its width being at least twice as large as an instruction length (See column 13, table 2: At least two-times the instruction length is prefetched);

means for performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded (See figure 4 and column 12, lines 7-14 and column 18, lines 57-62: The prefetch service block does the actual requesting for prefetches when appropriate. Prefetching is also taught to be able to be done, at the discretion of having ordinary skill in the art, at various stages of the pipeline of figure 4. The pipeline includes a decode stage), otherwise performing the prefetch request sequentially to prefetch instructions (See column 13, lines 13-17: The access controller can either issue an already prefetched instruction or request a prefetch); and

means for prefetching the branch target instruction when a branch is ensured to occur by executing the branch instruction (See column 12, lines 7-14: The prefetch service block does the actual requesting for prefetches when appropriate); and

means for ignoring the branch target instruction when a branch does not occur (See table 2 in column 13: A prefetch is suppressed if a branch is known not to occur).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7-8, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krueger et al (U.S. Patent # 6,195,735 B1), herein known as Krueger et al in view of Hanawa et al (U.S. Patent # 5,269,007), herein known as Hanawa et al.

As per **claims 7 and 16**, Krueger et al teaches both an instruction request control circuit (Access controller 22, see figures 1, 2, and 3) and a prefetch control circuit (Prefetch service block 80, see figure 3).

Krueger et al does not teach when a delayed branch instruction appears, a branch to occur following an instruction subsequent to the delayed branch instruction.

Hanawa et al teaches the use of a delay branch and delay slot (See column 10, lines 10-68: Describes the delay branch and delay slot), which increase performance and maximize efficiency by guaranteeing valid instructions while deciding whether branching is to be done or not.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Krueger et al to include the use of delay branch and delay slots.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Krueger et al by the teachings of Hanawa et al because the use of delay branches and delay slots help increase performance and maximize efficiency, which is a goal of Krueger et al (See column 1, lines 18-25).

As per **claims 8 and 17**, Krueger et al teaches a conditional branch instruction (See column 17, lines 30-33).

Krueger et al does not teach an unconditional branch instruction.

Hanawa et al teaches the use of an unconditional branch instruction (Also known as a jump instruction, see column 7, lines 7-10), which is also a basic instruction employed by many processor architectures.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Krueger et al to include the use of jump instructions.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Krueger et al to use an unconditional branch instruction, as taught by Hanawa et al, in order allows access to more memory addresses (See Hanawa et al, column 8, lines 10-13). Further, an unconditional branch instruction is a basic instruction of processor architectures.

9. Claims 3, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krueger et al (U.S. Patent # 6,195,735 B1), herein known as Krueger et al in view of Dean (U.S. Patent # 5,544,342), herein known as Dean.

As per **claims 3 and 12**, Krueger et al teaches a prefetch control circuit (Prefetch service block 80, see figure 3) which outputs to an instruction cache memory.

Krueger et al does not teach a control signal for canceling the prefetch request, which has been performed to prefetch the branch target instruction, when the branch does not occur, to thereby prevent an access to the main memory, the access being caused by a cache miss.

Dean teaches the canceling of instructions in the event of a branch is not taken (See column 72, lines 47-51).

Krueger et al's system may fetch wrong instructions in operation. Adding the control for canceling the unnecessary instruction will be desirable and certainly will increase the processing power of the Krueger et al's system.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Krueger et al to include the use of canceling fetch instructions, as taught by Dean, in order to prevent the processor from accessing invalid data and executing wrong instructions.

Conclusion

10. This is a continuation of applicant's earlier Application No. 10/686,638. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DONALD SPARKS
SUPERVISORY PATENT EXAMINER